Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **RESET 1**
2. **DATA 1**
3. **CLOCK 1**
4. **SET 1**
5. **Q1**
6. **N. Q1**
7. **GND**
8. **N. Q2**
9. **Q2**
10. **SET 2**
11. **CLOCK 2**
12. **DATA 2**
13. **RESET 2**
14. **VCC**

**.060”**

**9**

**8**

**7**

**6**

**12 11 10**

**3 4 5**

**13**

**14**

**1**

**2**

**.062”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: VCC**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .060” X .062” DATE: 3/16/18**

**MFG: MOTOROLA THICKNESS .010” P/N: 54HC74**

**DG 10.1.2**

#### Rev B, 7/1